

Notice of Allowability

Application No.

10/821,017

Examiner

My-Trang N. Ton

Applicant(s)

JIANG, JIAN H.

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amdt. filed 7/7/05.
2. ☒ The allowed claim(s) is/are 1-4, 7-11, 14-20.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date 6/27/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____

MY-TRANG NUTON
PRIMARY EXAMINER

9/19/05

Reasons for allowance

The following is an examiner's statement of reasons for allowance:

The present invention is drawn to a circuit for converting a signal from a low voltage domain to a high voltage domain utilizing a receiver (means for receiving), first – third transistors, at least one control transistor and a control structure (means for controlling, means for dividing, means for inverting, means for applying), or an inverted NAND gate, an inverter, first – fifth transistors recited in claims 1-4, 7-11, 14-20. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: **“controlling comprises applying the input signal to at least one control transistor operable to control at least one of the second and third transistors”, “dividing the input signal into two portions, wherein the first portion of the input signal is applied to the control transistor”, “applying the second portion of the input signal to a gate terminal of the first transistor”** in combination with the first – third transistors as recited in claim 1; **“applying the input signal to at least one control transistor operable to control at least one of the second and third transistors”, “means for dividing the input signal into two portions, wherein the first portion of the input signal is applied to the control transistor” “means for applying the second portion of the input to a gate terminal of the first transistor”** in combination with the first – third transistors as recited in claim 15; **“the inverted NAND gate”, “the inverter”, “the fourth – fifth transistors”** in combination with “the first – third transistors” as recited in claim 18.

The prior art references submitted by the applicant on IDS form received on 7/7/05 were reviewed and considered. These references appear to be the best references with respect to the claimed invention and closely matched most of the references found during the examiner's searches. However, as noted above, the limitations **"controlling comprises applying the input signal to at least one control transistor operable to control at least one of the second and third transistors"**, **"dividing the input signal into two portions, wherein the first portion of the input signal is applied to the control transistor"**, **"applying the second portion of the input signal to a gate terminal of the first transistor"** (claim 1); **"applying the input signal to at least one control transistor operable to control at least one of the second and third transistors"**, **"means for dividing the input signal into two portions, wherein the first portion of the input signal is applied to the control transistor"** **"means for applying the second portion of the input to a gate terminal of the first transistor"** (claim 15); **"the inverted NAND gate"**, **"the inverter"**, **"the fourth – fifth transistors"** (claim 18) are not disclosed. Therefore, the claims are patentably distinct over all these prior art references of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton
Primary Examiner
Art Unit 2816

September 12, 2005